



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,144	07/15/2003	Aphrodite Chen	COR 128	6077

  

7590 RABIN & BERDO, P.C. 1101 14th Street, N.W. Washington, DC 20005		01/17/2008
---	--	------------

  

EXAMINER ZAIDI, SYED	
-------------------------	--

  

ART UNIT 2616	PAPER NUMBER
------------------	--------------

  

MAIL DATE 01/17/2008	DELIVERY MODE PAPER
-------------------------	------------------------

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/619,144

Applicant(s)

CHEN, APHRODITE

Examiner

Syed Zaidi

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on Oct 26<sup>th</sup> 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) ✓
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## Detailed Action

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner

presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 1-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lu et al.**, (U.S. Patent # 7139267 B2) in view of **Juszkiewicz et al.** (U.S. Patent Application Publication # 2003/0172797 A1).

**Consider claim 1, Lu et al.**, discloses and shows a single chip Ethernet switch a multiple port single chip (column 1 lines 23-34) Ethernet switch comprising at least the following component parts: a physical layer entity (PHY) including a plurality of ports (column 3 lines 7-12) and are the ports (IC) with multiple ports); an address table for being written to and read out information (column 3 lines 35-50, figure # 5) to operate the plurality of ports (column 3 lines 57-

65, figure # 5). However **Lu et al.**, fails to disclose the test source address learning engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip, wherein said component parts of said Ethernet switch are formed on said single chip.

In the same field of endeavor of **Juszkiewicz et al.**, clearly shows and discloses test source address learning engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip, wherein said component parts of said Ethernet switch are formed on said single chip (paragraph 0149 lines 1-11, figure # 11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate test source address learning engine for performing a packet source address learning process under the daisy chain test mode to deliver

a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip, wherein said component parts of said Ethernet switch are formed on said single chip as taught by of **Juszkiewicz et al.**, with the method as disclosed by **Lu et al.**, for the purpose effectively queuing information by proper combination of daisy chain mode to deliver on single chip within the network architecture.

**Consider claim 2**, and as applied to claim 1 above,, as modified by **Juszkiewicz et al.**, clearly shows and discloses the switch further comprising an input for receiving the test packet (column 1 lines 35-40, figure # 1). This is done by monitoring all input IP packets destined to each switch and checking whether the source IP address of the input packet matches any of the CMP addresses. If there is a match, then conflict is declared (column 3 lines 35-54, figure # 1).

**Consider claim 3**, and as applied to claim 1 above, **Lu et al.**, as modified by **Juszkiewicz et al.**, clearly shows and discloses the

switch further comprising a packet generator for generating the test packet. Data packets are sent between the commander 100 and member switches (10-12) via the network connection (column 4 lines 5-15, figure # 6).

**Consider claim 4**, and as applied to claim 3 above, **Lu et al.**, as modified by **Juszkiewicz et al.**, clearly shows and discloses the switch further comprising a register for storing information of the test packet. This method has proven to be satisfactory in field tests (column 2 lines 19-36, figure # 2). With the commander switch at the center, all of the member switches may be added to the cluster at once. Wherein said component parts of said Ethernet switch are formed on said single chip (column 1 lines 23-34). However **Lu et al.**, fails to discloses the test source address learning engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip,

In the same field of endeavor of **Juszkiewicz et al.**, clearly shows and discloses test source address learning engine for performing a packet source address learning process under the daisy chain test mode (paragraph 0028 lines 10-13) to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip (paragraph 0142 lines 1-11) wherein said component parts of said Ethernet switch are formed on said single chip (paragraph 0149 lines 1-5, figure # 11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate test source address learning engine for performing a packet source address learning process under the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip, wherein said component parts of said Ethernet switch are formed on said single chip as taught by of **Juszkiewicz et al.**, with the method as disclosed by **Lu et al.**, for the purpose effectively queuing

information by proper combination of daisy chain mode to deliver on single chip within the network architecture.

**Consider claim 5**, and as applied to claim 1 above, **Lu et al.**, as modified by **Juszkiewicz et al.**, clearly shows and discloses the switch further comprising a verification unit for verifying the test packet (column 2 lines 19-36, figure # 2) and monitoring logic for monitoring a source IP address of input IP packets received by said member network device. Ethernet switch (10) also includes a frame buffer memory (column 2 lines 13-18, figure # 2) for each port, a source address table memory, discovery protocol logic, learning logic, forwarding logic, packet redirection logic, and a configuration and management interface as mention (column 3 lines 22-29, figure # 4).

**Consider claim 6**, and as applied to claim 1 above, **Lu et al.**, as modified by **Juszkiewicz et al.**, clearly shows and discloses the further comprising an output for sending out the test packet

(column 1 lines 35-54) and clearly explain some other IP station can be using the same address as an automatically assigned CMP address. Thus, both the commander switch and the member switches constantly check for conflicts, and in case of a conflict a new CMP address is generated. **Lu et al.**, further explain in a block diagram illustrating the CRC (cyclic redundancy check) packet format according to aspects of the present invention (column 14 lines 13-18, figure # 13).

**Consider claim 7**, and as applied to claim 1 above, **Lu et al.**, as modified by **Juszkiewicz et al.**, clearly shows and discloses the switch, wherein the test source address learning engine includes a writing apparatus for writing a set of initial addresses to the address table under the daisy chain test mode. (**Lu et al.**, explain when a member switch is added to a cluster, the commander generates a unique cluster IP address and assigns it to the member switch. The commander's cluster IP address is also passed to the member switch. These cluster IP addresses are dynamically assigned. When the commander finds a conflict with one of the assigned cluster IP

addresses then the commander resolves the conflict by selecting another cluster IP address when a member switch is added to a cluster as shown in (column 14 lines 13-18, figure # 13) the commander generates a unique cluster IP address and assigns it to the member switch. The commander's cluster IP address is also passed to the member switch. These cluster IP addresses are dynamically assigned. Then the switches that are directly connected to the commander switch may be added first. However **Lu et al.**, fails to disclose the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip.

In the same field of endeavor of **Juszkiewicz et al.**, clearly shows and discloses the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip (paragraph 0028 lines 10-13) to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip (paragraph 0142 lines 1-11) wherein said

component parts of said Ethernet switch are formed on said single chip (paragraph 0149 lines 1-5, figure # 11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate discloses the daisy chain test mode to deliver a test packet through the plurality of ports progressively from a start transmission port to a stop receiving port to test the chip, as taught by of **Juszkiewicz et al.**, with the method as disclosed by **Lu et al.**, for the purpose effectively queuing information by proper combination of daisy chain mode to deliver on single chip within the network architecture.

**Consider claim 8**, and as applied to claim 1 above, **Lu et al.**, as modified by **Juszkiewicz et al.**, clearly shows and discloses the switch wherein the packet source address learning process sets a packet destination address as a next port (column 1 lines 34-54). (**Lu et al.**, explain the total number of ports available for connecting to workstations or other network devices on each LAN switch is diminished due to the dedicated inter switch connections that are necessary to implement the cascaded configuration. The source and

destination addresses of Ethernet packets under control of the configuration and management interface and forwards them to other network devices in a cluster configuration (column 4 lines 2-5, figure # 6)

**Claims 9-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Duvvury** (U.S. Patent Application Publication # 2005/0213560 A1) in view of **Lu et al.**, (U.S. Patent Application Publication # 7139267 B1).

**Consider claim 9, Duvvury** disclose and show a daisy chain test for (paragraph 0075 lines 1-9, figure # 9) a single chip Ethernet switch integrated with a physical layer entity including a plurality of ports (paragraph 0024 lines 5-25, figure # 3), the switch having an address table for being written to and read out information to operate the plurality of ports (paragraph 0024 lines 1-5, figure # 3), the test comprising the steps of: connecting each of the plurality of ports to a respective passive loop-back device; selecting a start transmission port and a stop receiving port from the plurality of ports (paragraph 0027 lines 1-10, figure # 4); supplying a test packet to the start

transmission port; and proceeding a packet source address (paragraph 0023 lines 1-15, figure # 3) learning process for delivering the test packet from the start transmission port to the stop receiving port progressively, wherein the step of proceeding employs a source address learning engine with a daisy chain testing function (paragraph 0067 lines 1-5, figure # 9); and determining a test result by verifying a last received packet at the stop receiving port.

However **Duvvury** fails to disclose the wherein said component parts of said Ethernet switch are formed on said single chip.

In the same field of endeavor of **Lu et al.**, clearly shows and discloses wherein said component parts of said Ethernet switch are formed on said single chip (paragraph 0149 lines 1-11, figure # 11).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate as taught by of **Lu et al.**, with the method as disclosed by **Duvvury** for the purpose effectively queuing information by proper combination of daisy chain mode to deliver on single chip within the network architecture.

**Consider claim 10**, and as applied to claim 9 above, **Duvvury** as modified by **Lu et al.**, disclose the test further comprising inputting the test packet to the switch (paragraph 0028 lines 1-10, figure # 5).

**Consider claim 11**, and as applied to claim 9 above, **Duvvury** as modified by **Lu et al.**, disclose the test further comprising generating the test packet in the switch (paragraph 0018 lines 1-10, figure # 2) for Ethernet access to packet-based services (paragraph 0023 lines 1-15, figure # 3).

**Consider claim 12**, and as applied to claim 9 above, **Duvvury** as modified by **Lu et al.**, disclose the test further comprising verifying the test packet after the stop receiving port (paragraph 0059 lines 1-15, figure # 2).

**Consider claim 13**, and as applied to claim 12 above, **Duvvury** as modified by **Lu et al.**, disclose the test further comprising sending out the test packet from the stop receiving port (paragraph 0021 lines 1-16, figure # 4). **Duvvury**, clearly explain in an Ethernet

protocol network having a plurality of platforms, with at least a first second platforms serving a group of members, a method of routing at least one frame from at least one sending member of group served by a first platform to at least one receiving member of the served by a second platform, comprising the steps (paragraph 0018 lines 1-10, figure # 2-B).

**Consider claim 14**, and as applied to claim 9 above, **Duvvury** as modified by **Lu et al.**, disclose the test wherein the learning process sets a packet destination address as a next port (paragraph 0004 lines 1-10, figure # 1). **Duvvury** clearly explain that an Ethernet Metropolitan Area Network provides connectivity to one or more customer premises to packet-bases services, such as ATM, Frame Relay, or IP while advantageously provides a mechanism for assuring security and regulation of customer traffic (paragraph 0012 lines 1-10, figure # 1).

### **Response to Arguments**

Applicant's arguments with respect to claims 1- 14 have been considered but are moot in view of the new ground(s) of rejection.

Claims 1 and 9 are amended.

Claims 1-14 are rejected.

Note: Applicants, amendment necessitated a new ground of rejection.

### **Conclusion**

Any response to this Office Action should be **faxed to** (571) 273-8300  
**or mailed to:**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**Hand-delivered responses** should be brought to

Customer Service Window  
Randolph Building  
401 Dulany Street  
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Syed S.Zaidi whose

telephone number is (571) 270-1779. The examiner can normally be reached on Monday - Friday 8:00-5:00 EST.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema S.Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the

Application/Control  
Number: 10/619,144  
Art Unit: 2616

Page 18

receptionist/customer service whose telephone number is (571) 272-  
2600.

*Syed S. Zaidi*  
Syed S. Zaidi  
S.Z./sz

January 10th, 2008.

*Seema S. Rao*  
SEEMA S. RAO 1/14/08  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600